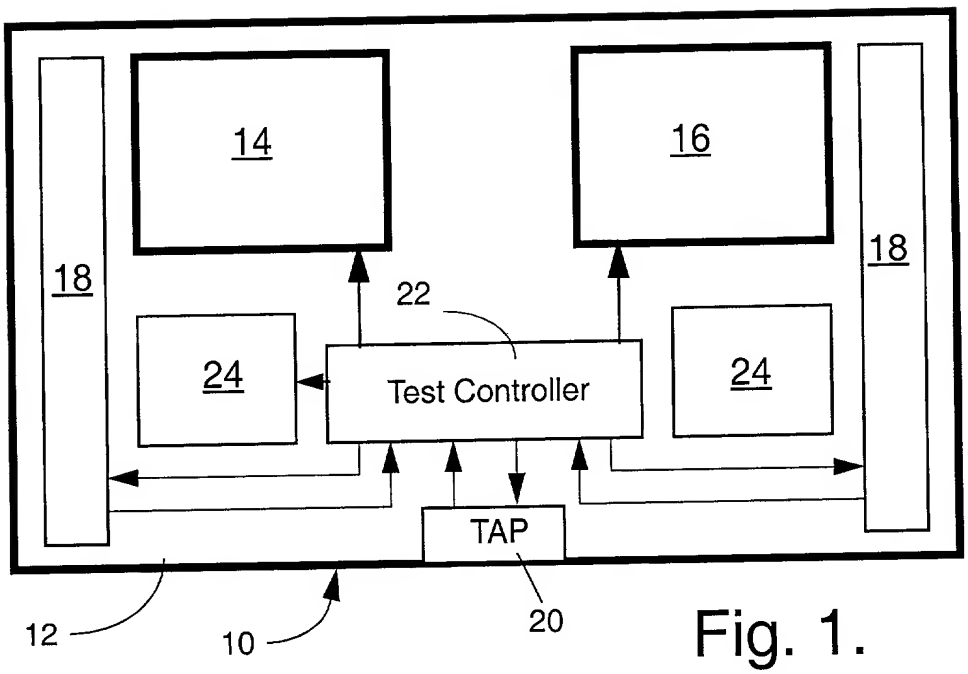


Fig. 1.

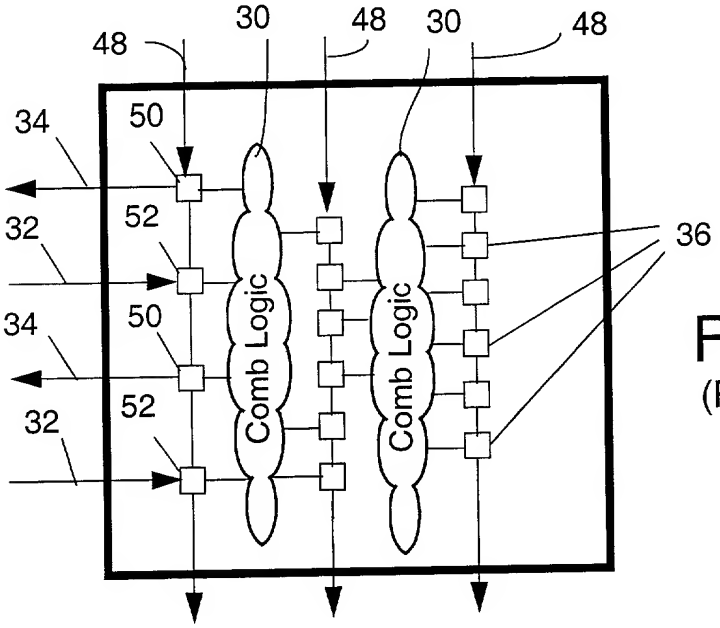


Fig. 2.
(Prior Art)

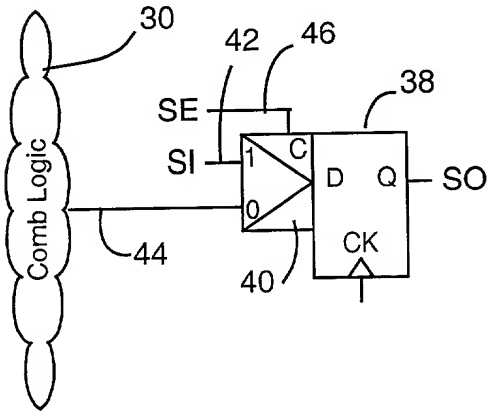


Fig. 3.
(Prior Art)

Fig. 4.

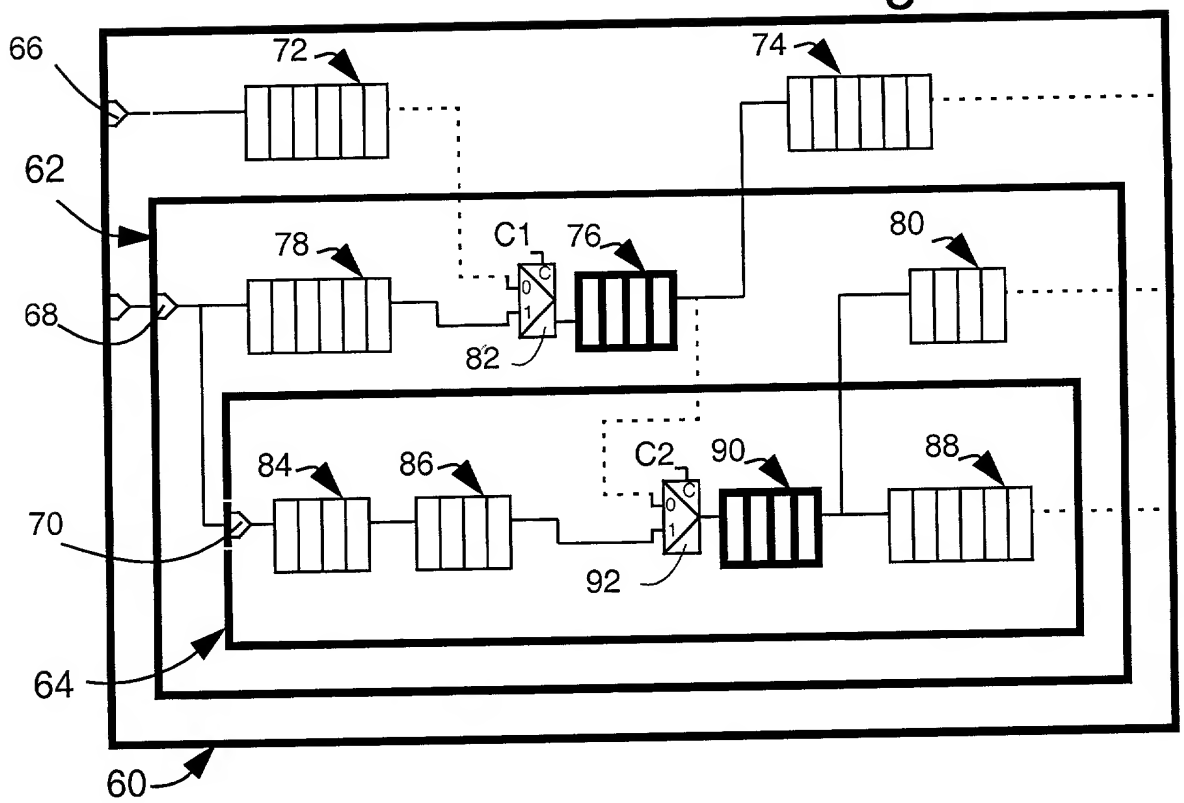

66
72
74
62
78
C1
76
80
68
82
84
86
C2
90
88
70
92
64
60

Fig. 5.

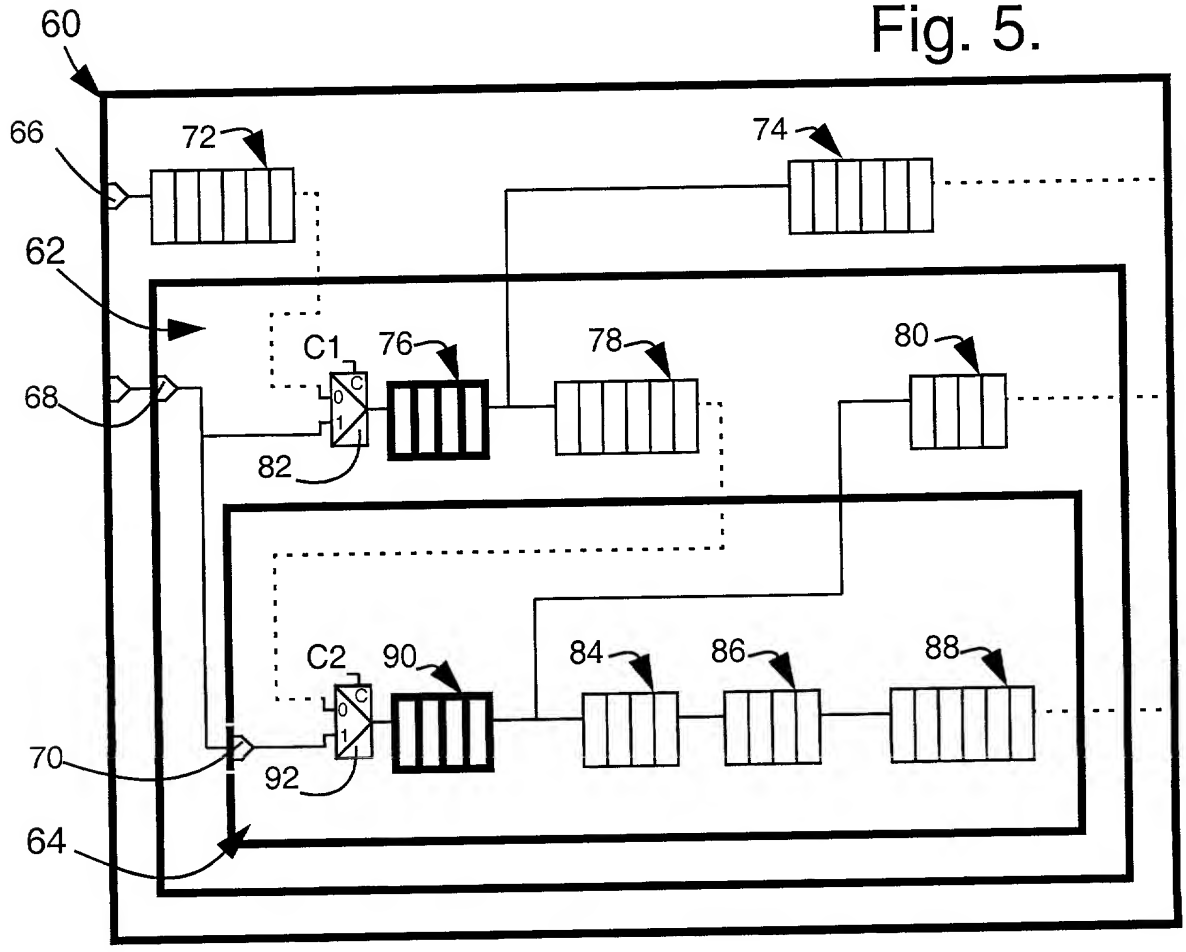

60
66
72
74
62
C1
76
78
80
68
82
C2
90
84
86
88
70
92
64

Fig. 6.

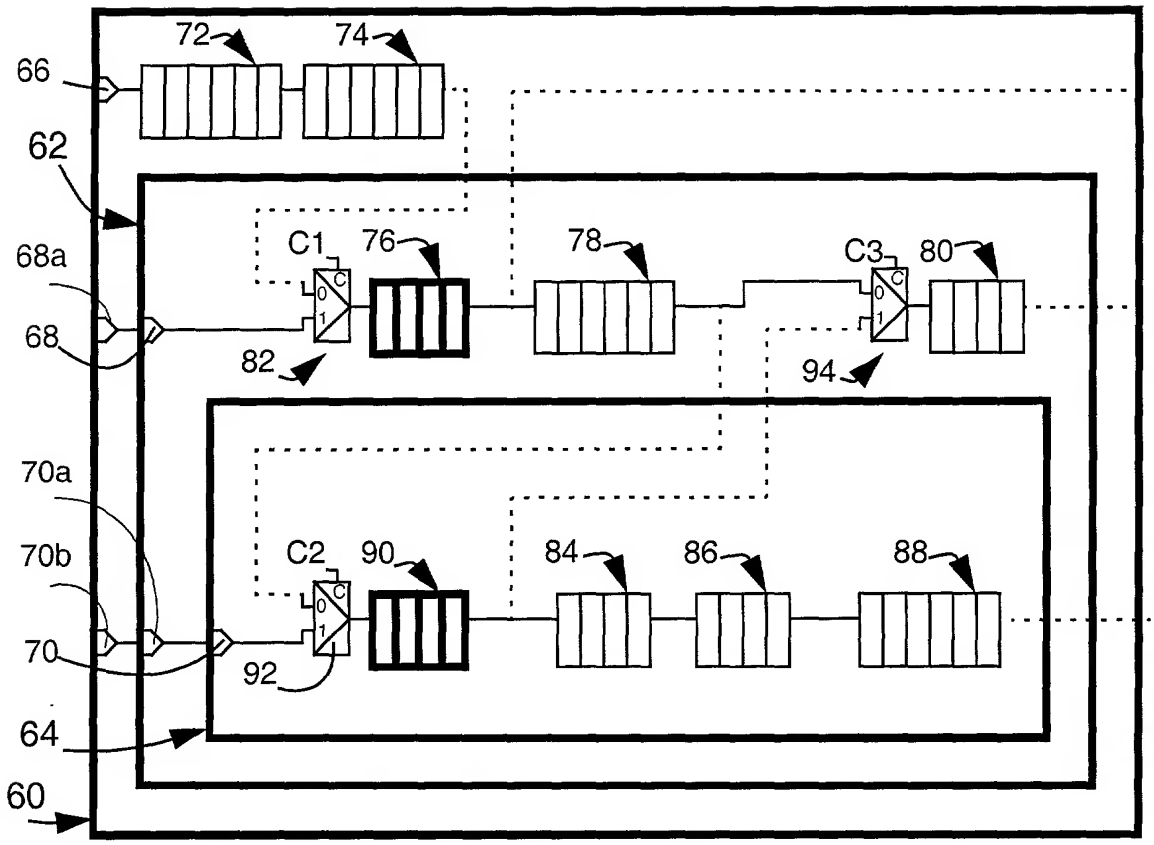
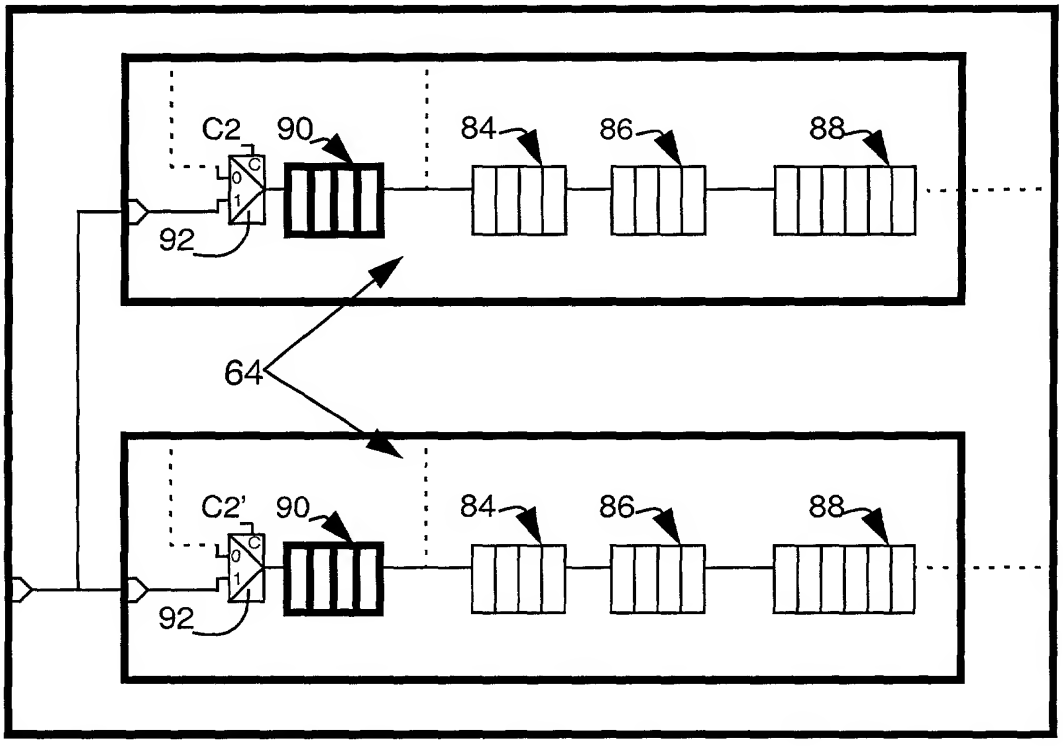

72
74
66
62
C1
76
78
C3
80
68a
68
82
94
70a
C2
90
84
86
88
70b
70
92
64
60

Fig. 7.


C2
90
84
86
88
92
64
C2'
90
84
86
88
92

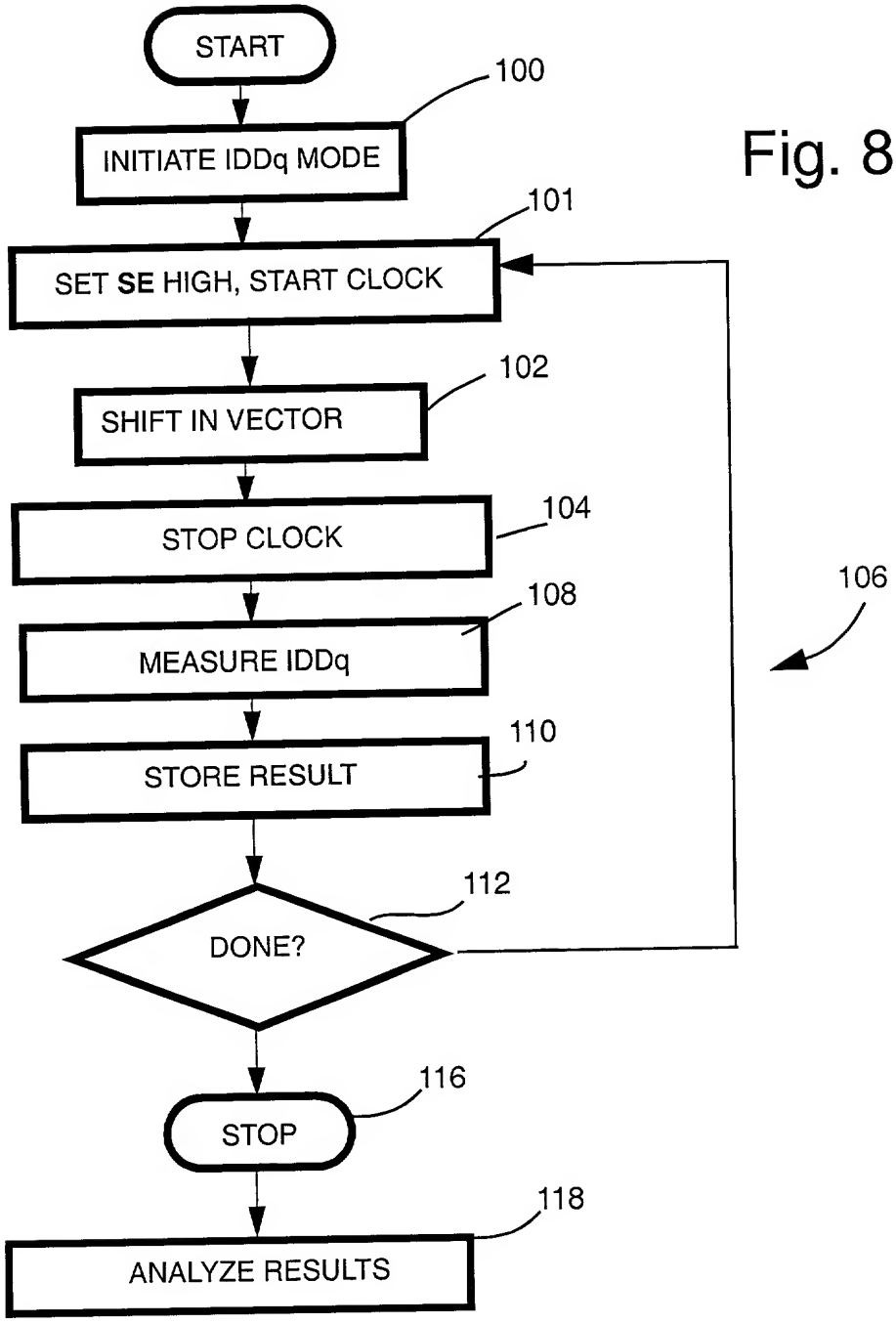

START
100
INITIATE IDDq MODE
101
SET SE HIGH, START CLOCK
102
SHIFT IN VECTOR
104
STOP CLOCK
108
MEASURE IDDq
110
STORE RESULT
112
DONE?
106
116
STOP
118
ANALYZE RESULTS

Fig. 8.

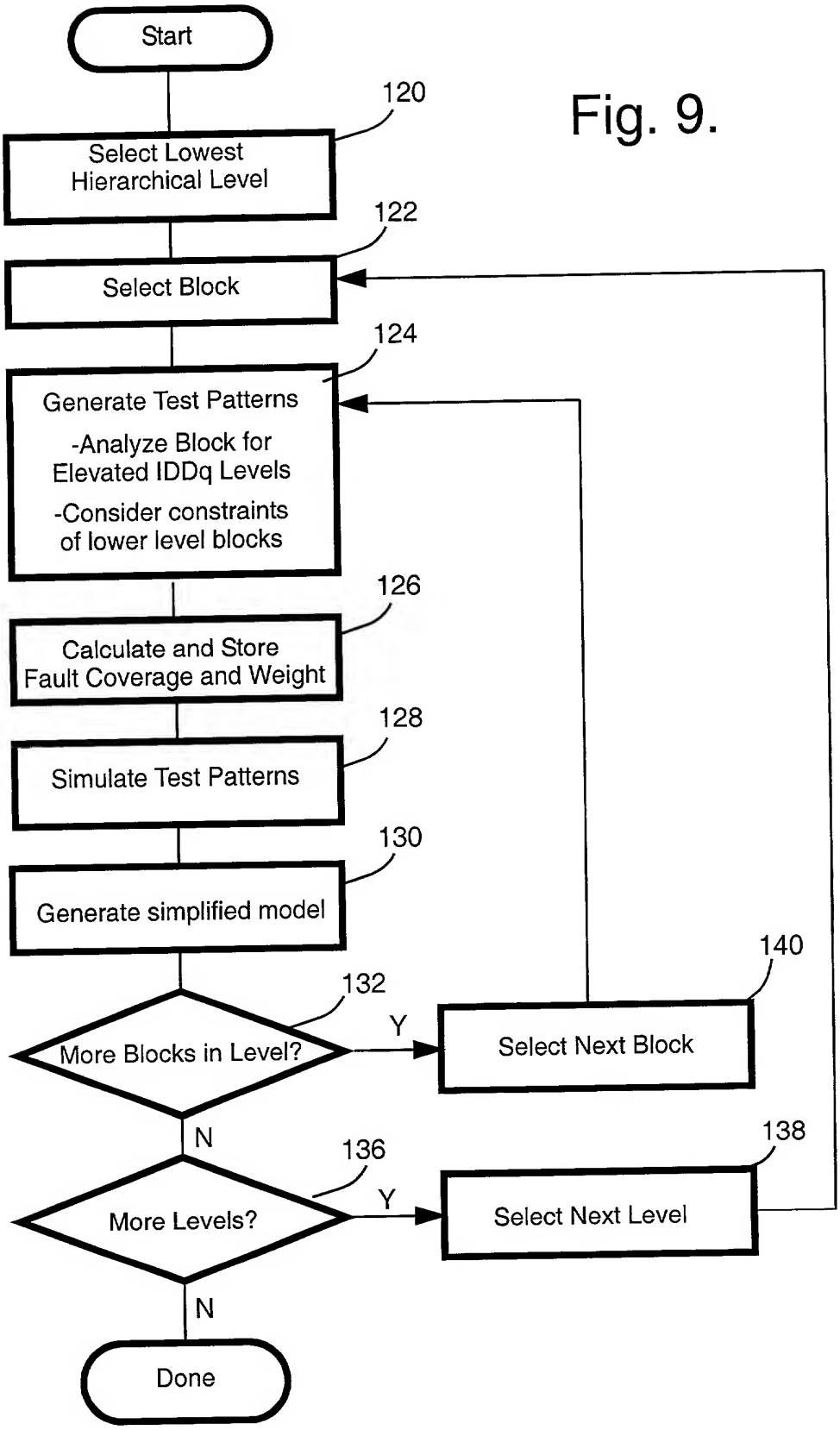
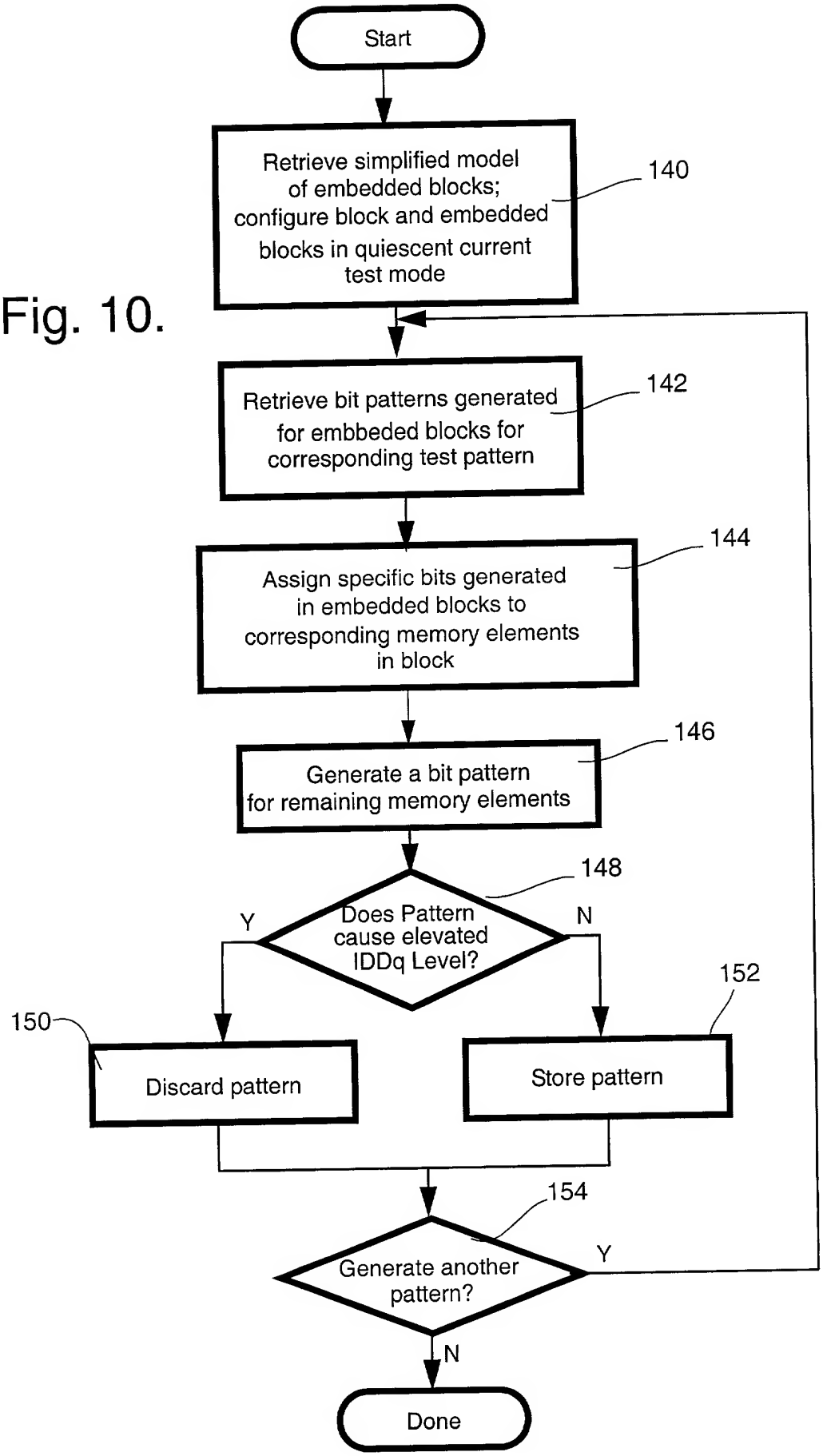

Start
120
Select Lowest Hierarchical Level
122
Select Block
124
Generate Test Patterns
-Analyze Block for Elevated IDDq Levels
-Consider constraints of lower level blocks
126
Calculate and Store Fault Coverage and Weight
128
Simulate Test Patterns
130
Generate simplified model
132
More Blocks in Level?
Y
140
Select Next Block
N
136
More Levels?
Y
138
Select Next Level
N
Done

Fig. 9.

Fig. 10.


Start
Retrieve simplified model of embedded blocks; configure block and embedded blocks in quiescent current test mode
140
Retrieve bit patterns generated for embbeded blocks for corresponding test pattern
142
Assign specific bits generated in embedded blocks to corresponding memory elements in block
144
Generate a bit pattern for remaining memory elements
146
Does Pattern cause elevated IDDq Level?
148
Y
N
Discard pattern
150
Store pattern
152
Generate another pattern?
154
Y
N
Done

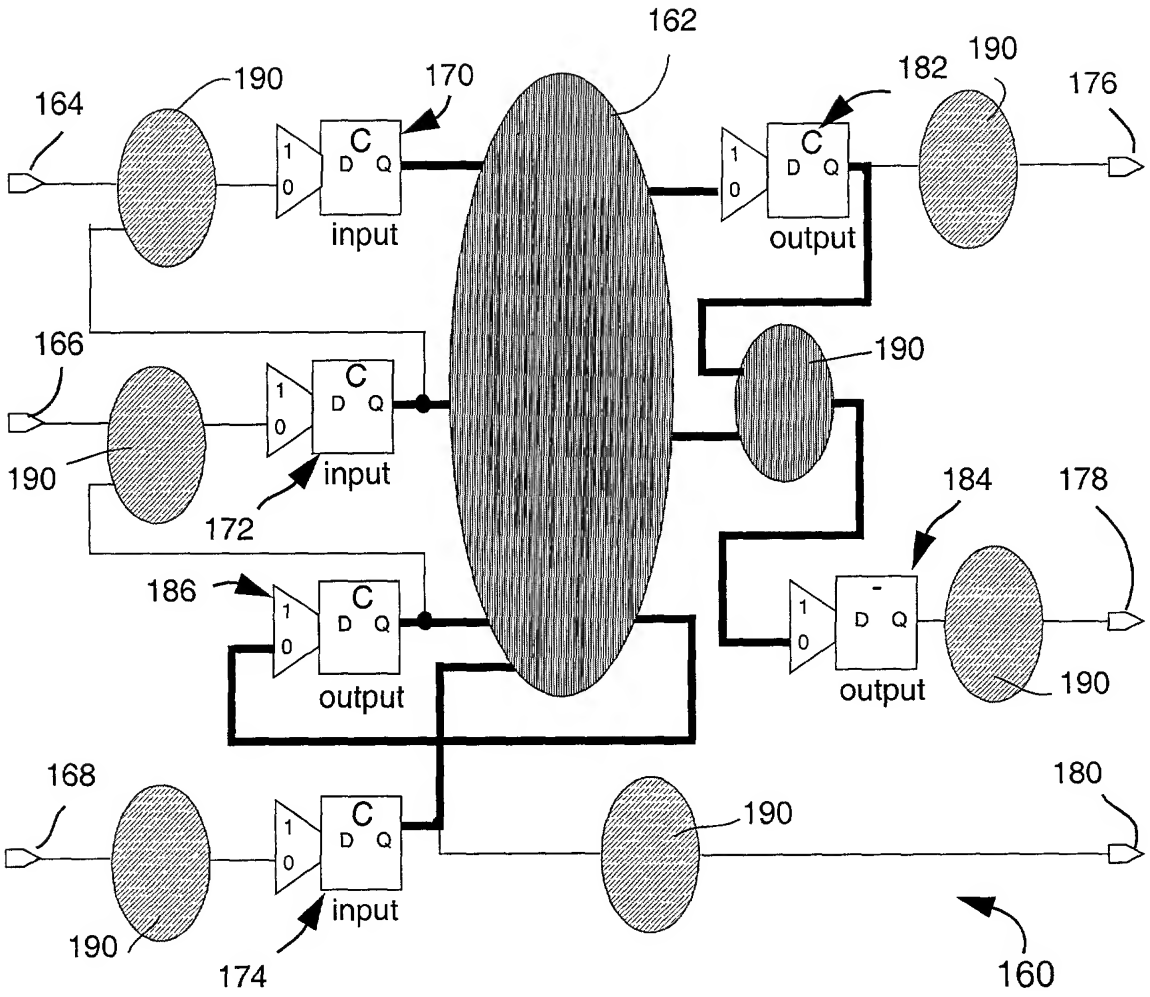

162
164
190
170
182
190
176
input
output
166
190
190
184
178
172
input
186
output
output
190
168
180
190
190
input
174
160
internal logic
peripheral logic

Fig. 11.

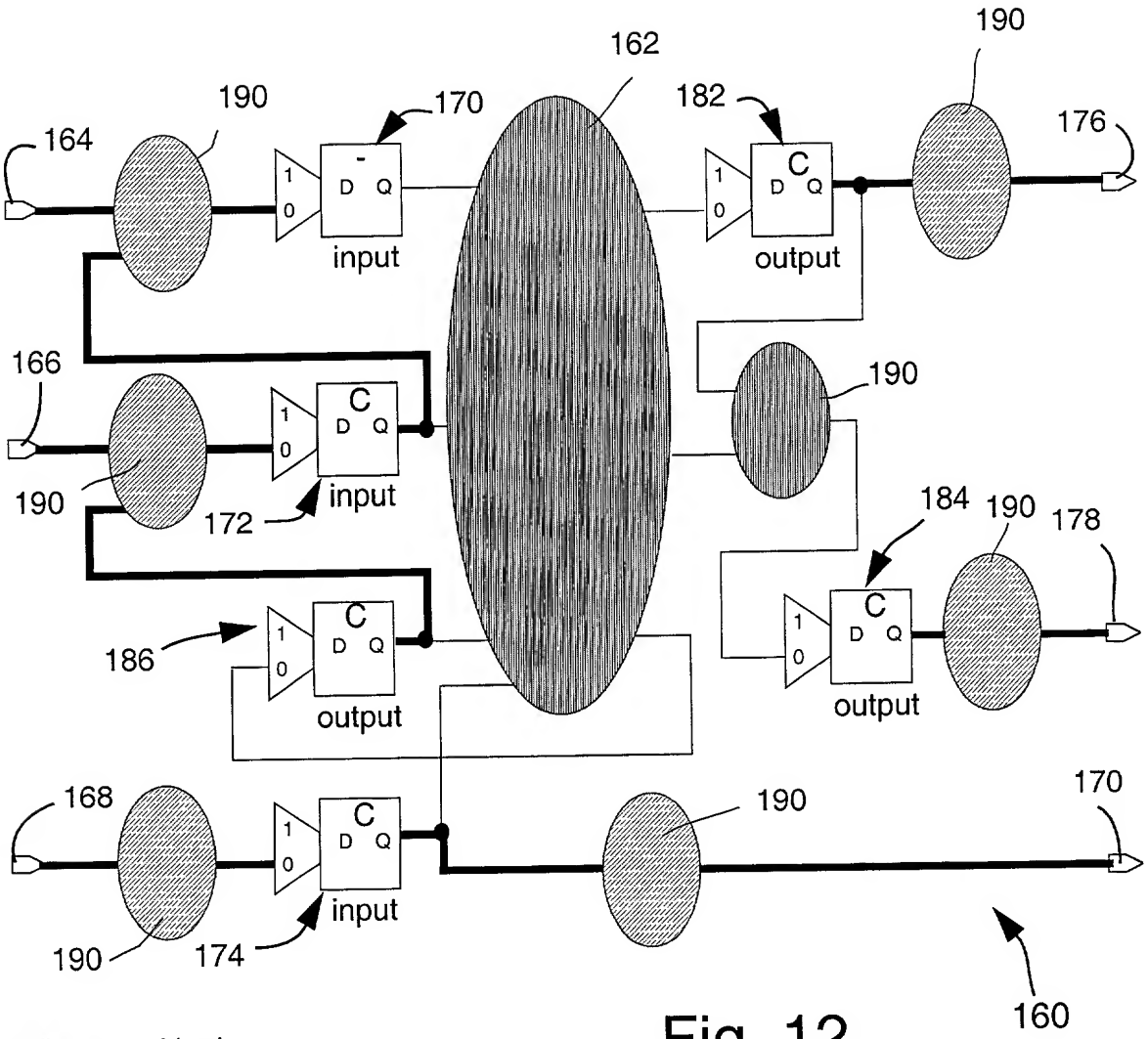

162
190
190
170
182
176
164
input
output
166
190
190
172
input
184
190
178
186
output
output
168
190
170
190
174
input
160
internal logic
peripheral logic

Fig. 12.

Fig. 13.

TABLE 1. IDDq patterns for configuration of figure 11

Fxxx	Fxxy	F170	F172	F174	F182	F184	F186	Fxxz	Fxxt
0	1	1	X	0	0	X	1	0	1
1	1	0	1	X	1	X	0	0	0
0	X	X	0	1	X	1	X	1	0
X	0	0	0	1	1	0	0	X	1
1	0	1	X	X	X	X	X	0	X
1	0	1	X	X	X	X	X	0	X

TABLE 2. IDDq patterns for configuration of figure 12

Fyyy	Fyyx	Fyyz	F172	F174	F182	F184	F186	Fyyt	Fyyu	Fzzx	Fzzy
1	1	0	1	0	0	0	1	0	1	1	0
1	1	0	1	0	1	1	0	0	0	0	1
0	X	X	0	1	0	1	1	1	0	X	1
X	0	0	0	1	1	0	0	X	1	0	X
0	1	0	1	0	0	0	1	0	0	1	1
1	0	X	0	0	1	1	1	X	1	0	0

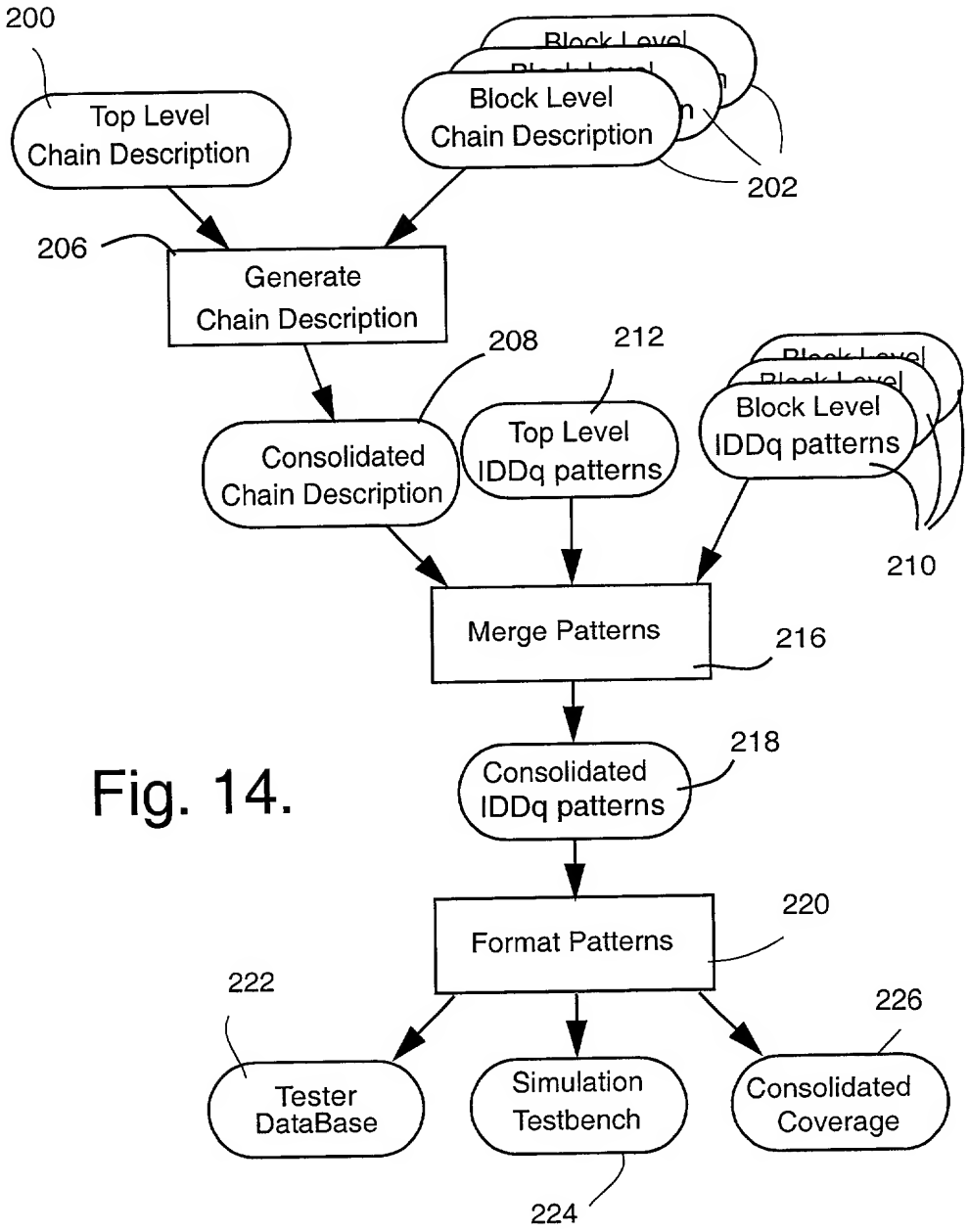
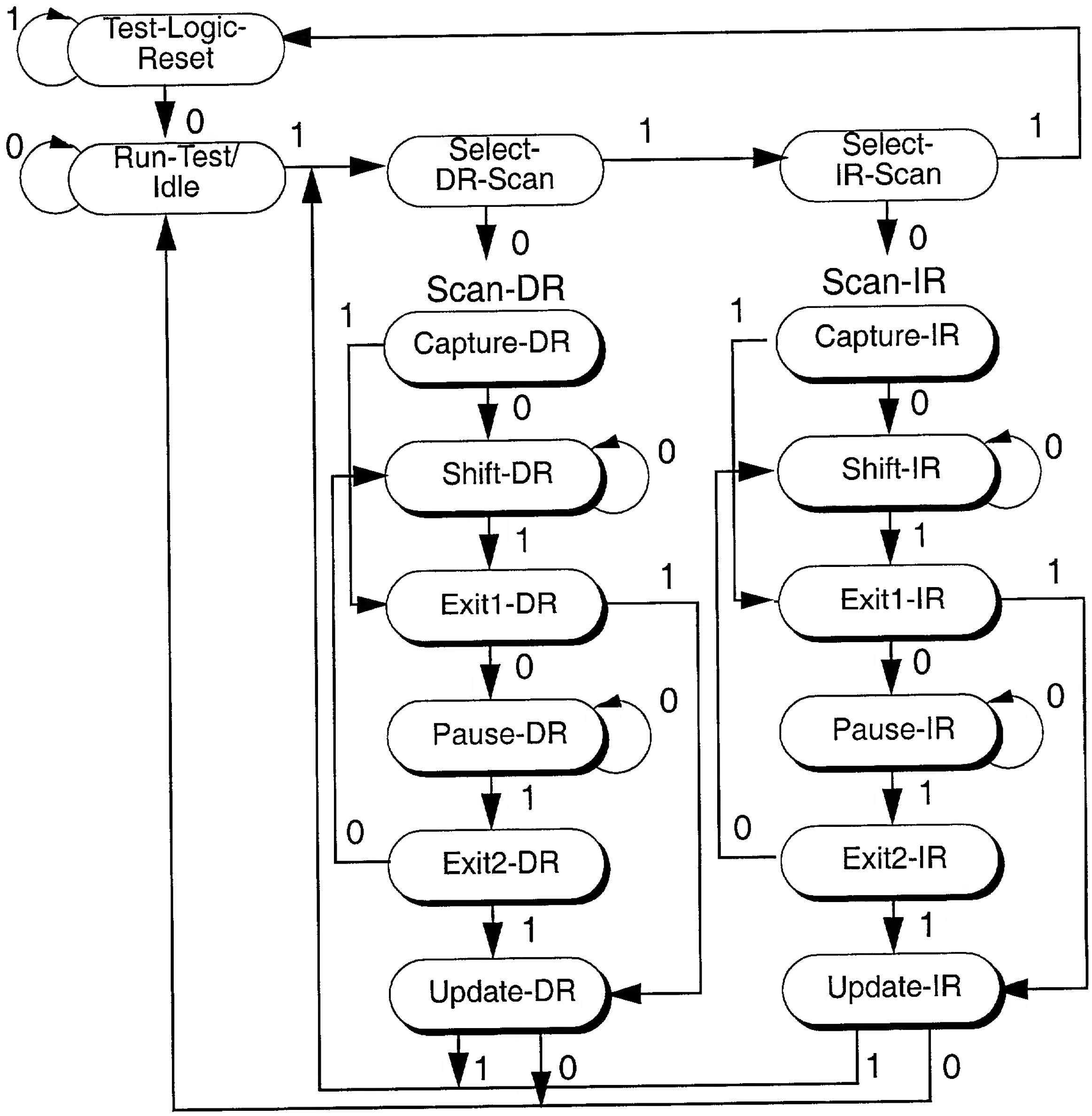

200
Top Level
Chain Description
Block Level
Chain Description
202
206
Generate
Chain Description
208
212
Consolidated
Chain Description
Top Level
IDDq patterns
Block Level
IDDq patterns
210
Merge Patterns
216
218
Consolidated
IDDq patterns
220
Format Patterns
222
226
Tester
DataBase
Simulation
Testbench
Consolidated
Coverage
224

Fig. 14.



NOTE: The values adjacent to each state transition correspond to *TMS*.

Fig. 15.
(Prior Art)